

## **REMARKS**

Applicant respectfully requests reconsideration of this application, as amended, and consideration of the following remarks. Claims 1, 12 and 15 have been amended. Claims 2-4 and 13 have been previously canceled. Claims 1, 5-12 and 14-18 remain pending.

Claims 1-18 stand rejected under 35 U.S.C. 102(b). Applicant traverses this rejection as set forth in more detail below. Applicant thanks the Examiner for withdrawing the prior rejections under 35 USC 101 and 112.

### **Amendments**

#### ***Amendments to the Claims***

Applicant has amended the claims to more particularly point out what Applicant regards as the invention. No new matter has been added as a result of these amendments.

### **Rejections**

#### ***Rejections under 35 U.S.C. §102(b)***

Claims 1-18 stand rejected under 35 U.S.C. § 102(b) as being unpatentable over Hennessey et al (Computer Architecture: A quantitative Approach). Applicant respectfully traverses the rejection.

Hennessey teaches pipelining instructions and their hazards (e.g., stalls, etc.) that can occur in a pipeline.

Applicant's system and method provide that each swap is processed as a SAVE instruction and a RESTORE instruction in two consecutive clock cycles at all times and therefore providing a constant two clock cycle latency. Applicant's invention includes circuitry and logic that achieves a flop function to complete the swap decoding without introducing additional clock cycles in the critical path. Immediately subsequent swaps will also have a constant two clock cycle latency.

Hennessey's MOVI2S, MOVS2I are not the same as Applicant's Move A <=> Move B as Applicant's SAVE might move contents of Active register to any one

of 8 or 4 window registers and Applicant's RESTORE might move contents of a different window register to the active register.

Applicant's method of executing the SAVE and RESTORE instructions provide a ***constant latency*** and ability to launch swaps ***every*** clock cycle. SAVE and RESTORE for the same SWAP happen in two consecutive clock cycles. Hence each SWAP MUST TAKE TWO CLOCK CYCLES. Hence a constant latency of two clock cycles (for example: RESTORE for SWAP A, SAVE for SWAP B can happen simultaneously) is achieved by internal pipelining of swap instructions and throughput every cycle to launch a new swap instruction.

Hennessey's MOVI2S, MOVS2I will not have a constant latency as described and claimed herein. Hennessey's MOVI2S, MOVS2I and any immediately subsequent move instructions will have a progressive latency that progressively gets worse as described in Applicant's paragraphs 4-6 and Figure 1A-1B. Hennessey does not teach nor even suggest how to maintain a constant latency.

As to claims 1, 12 and 15, the Hennessy reference does not teach nor even suggest a pipeline architecture or a method for processing a plurality of swap requests including receiving a first swap request in a pipeline wherein the first swap request requests swapping active contents of a active register window with a first contents from a first register and executing the first swap request. Executing the first swap request includes executing a first save operation wherein the active contents of the active register window is saved to corresponding register and executing a first restore operation, wherein the first contents of the first register are restored to the active register window. The method also includes receiving a second swap request in the pipeline immediately subsequent to the first swap request, wherein the second swap request requests swapping the first contents in the active register window with a second contents from a second register. The first register is examined to determine if the first register is a same register as the second register. The second swap request is executed if the first swap request and the second swap request do not swap the same register. Executing the second swap request includes executing a second save operation wherein the first contents of the active register window is saved to first register at substantially simultaneously with the executing the first restore operation

and executing a second restore operation, wherein the second contents of the second register are restored to the active register window, wherein the first swap request and the second swap request have a constant latency.

The Hennessey reference does not teach or even suggest each and every limitation as recited in claims 1, 12 and 15.

Accordingly, Applicant respectfully submits that Applicant's invention as claimed in claims 1, 12 and 15 and those claims that depend from one of claims 1, 12 and 15 are patentable over the Hennessey reference, and respectfully request the withdrawal of the rejection under 35 U.S.C. § 102(b).

### **SUMMARY**

In view of the foregoing amendments and remarks, Applicant respectfully submits that the pending claims are in condition for allowance. Applicant respectfully requests reconsideration of the application and allowance of the pending claims.

If the Examiner determines the prompt allowance of these claims could be facilitated by a telephone conference, the Examiner is invited to contact George B. Leavell at (408) 749-6900, ext 6923.

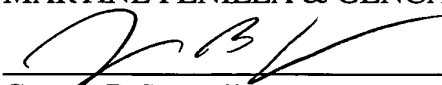
### **Deposit Account Authorization**

Authorization is hereby given to charge our Deposit Account No. 50-0805 (Ref # SUNMP351) for any charges that may be due or credit our account for any overpayment. Furthermore, if an extension is required, then Applicant hereby requests such extension.

Respectfully submitted,

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